REMARKS

Favorable reconsideration of this application, in light of the following discussion and in view of the present amendment, is respectfully requested.

Claims 1, 3 and 7-9 are cancelled. Claims 2 and 4 are amended. Claims 2 and 4-6 are pending in the application.

Entry of Amendment under 37 C.F.R. § 1.116

The Applicant requests entry of this Rule 116 Response because: the amendments were not earlier presented because the Applicant believed in good faith that the cited references did not disclose the present invention as previously claimed; and the amendment does not significantly alter the scope of the claim and places the application at least into a better form for purposes of appeal.

The Manual of Patent Examining Procedures (M.P.E.P.) sets forth in Section 714.12 that "any amendment that would place the case either in condition for allowance or in better form for appeal may be entered." Moreover, Section 714.13 sets forth that "the Proposed Amendment should be given sufficient consideration to determine whether the claims are in condition for allowance and/or whether the issues on appeal are simplified." The M.P.E.P. further articulates that the reason for any non-entry should be explained expressly in the Advisory Action.

I. Rejection under 35 U.S.C. § 102

In the Office Action, at page 6, numbered paragraph 3, claims 1-9 were rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 5,524,217 to Sone et al. This rejection is respectfully traversed. Claims 1, 3 and 7-9 were cancelled. The features of claims 1 and 3 were incorporated into claims 2 and 4.

Claims 2 and 4

Sone does not discuss or suggest:

> switching control means for switching an output state of said output means;
>
> output means for switching between a first state in which the system outputs a signal state of the wired OR signal line and a second state in which the system outputs a negate state of the wired OR signal line, and outputting either state to the other system; and
>
> an assert mechanism that maintains the wired OR signal line in an

> asserted state in response to an asserted state transferred by the output means of the other system;
>
> wherein said switching control means comprises a register controlled by a processor in the system, and said output means comprises: a mask mechanism which switches to said first state when the register indicates a predetermined value and which switches to the second state when the register indicates another value; and a transmission mechanism that transfers an output from said mask mechanism to the other system,

as recited in amended independent claim 2, and does not discuss or suggest:

> switching and controlling means for switching the output said switching and outputting means;
>
> switching and outputting means for switching between the first state where the signal state transmitted by the output means in the other system is output and the second state where negate state is output, and outputting the switched state; and
>
> an assert mechanism that switches the wired OR signal line between an asserted state or a negate state according to the output state of said switching and outputting means;
>
> wherein said switching and controlling means is composed of a register controlled by a processor in the system, and said switching and outputting means is composed of a mask mechanism which switches to the first state when said register has a predetermined value and switches to the second state when the register has a value other than the predetermined value,

as recited in amended independent claim 4.

The present invention as set forth in claim 2, for example, is directed to a device for transmitting a wired OR signal between two systems. Each system includes an output means for switching between two states – one in which the system outputs a signal state and one in which the system outputs a negate state – and outputting the state to the other system. The output means includes a mask mechanism which switches to the first state when the register indicates a predetermined value and which switches to the second state when the register indicates another value and a transmission mechanism that transfers an output from the mask mechanism to the other system. A switching control means, which is a register, is used to switch an output state of the output means, and an assert mechanism maintains the wired OR signal line in an asserted state in response to an asserted state transferred from the other system as a result of a system side device processing.

Sone discusses that when a peripheral device (an adapter) requests an interrupt for an MPU, the -IRQn line assigned to that device is driven to its low state, then the MPU executes a corresponding interrupt processing routine. After the processing routine is terminated, in Sone,

the MPU makes notification of an end of interrupt to the adapter of the peripheral device to drive the -IRQn line to its high state and the interrupt processing routine is terminated. Sone discusses that when an -IRQn line is driven to its low state by a peripheral device in one system, the signal is transferred to the other system to drive the corresponding -IRQn line to its low state by the IRQ processor and if the IRQ processor in the second system echoes back the low state of the -IRQn line of the second system, the -IRQn line of the first system is driven low by the IRQ processor as well as the peripheral device, thus the -IRQn lines of both system are driven low permanently. Sone discusses using shadow and shadow-shadow registers to resolve the problem of echoes providing the lock-up effect.

In Sone, as the adapter of the -IRQn line of the primary system is toggled to the low state, the wired-OR -IRQn line goes low, an IRQ packet is sent to the secondary system, which toggles the secondary shadow register from the high state to the low state, returning an ACK from the secondary system to the primary system, and toggling the primary shadow-shadow register from the high state to the low state. Then the secondary -IRQn line is similarly toggled to the low state, but as the secondary shadow register is already low, no IRQ packet is sent to the primary system as the secondary -IRQn line is toggled to the low state. Further, in Sone, the wired-OR -IRQn line goes high as the adapter toggles the -IRQn line from the low to high state, and an IRQ packet is sent from the primary system to the secondary system, so the secondary register is toggled from the low state to the high state. In response to the toggle, the secondary system returns an ACK to the primary system, so that the primary shadow-shadow register is toggled from the low state to the high state. Then the secondary -IRQn line also is turned from the low state to the high state in response to the toggle of the secondary show register, but since the secondary shadow-shadow register is in its high indication state, or the primary shadow register is in the high indication state, no IRQ packet is sent to the primary system is response to the toggle of the secondary -IRQn line.

While Sone does discuss that the states of -IRQn lines from each of the systems can be toggled from low to high states, Sone does not suggest a "switching control means for switching an output state of said output means," and does not suggest that "said switching control means comprises a register controlled by a processor in the system, and said output means comprises: a mask mechanism which switches to said first state when the register indicates a predetermined value and which switches to the second state when the register indicates another value; and a transmission mechanism that transfers an output from said mask mechanism to the other system," as recited in amended independent claim 2. Sone makes use of shadow registers and shadow-shadow registers that are toggled in response to reception of an IRQ

packet or reception of an ACK. The sending of packets or ACK toggles each of the shadow registers and shadow-shadow registers in Sone such that the registers may indicate the state of the other system. Further, when the registers are toggled, the -IRQn line is also toggled.

Sone does not suggest that a switching control means, which is a register controlled by the processor, switches the output state of output means, as set forth in claim 2. The registers in Sone are toggled based on the reception of an IRQ packet or an ACK, but are not used to switch an output state of an output means. Further, Sone does not suggest that a mask mechanism and a transmission mechanism are an output means that switches between a first state in which the system outputs a signal state of the wired OR signal line and a second state in which the system outputs a negate state of the wired OR signal line and outputs either state. The present invention, in contrast, makes use of a mask mechanism that switches to a first state or a second state based on the value indicated in the register. Sone discusses that, for example, when the shadow register of the secondary system is toggled from high to low, an ACK is then returned from the secondary system to the primary system, so the primary shadow-shadow register is toggled. Sone does not suggest that the shadow register is a switching control means that switches the state of an output means. When the shadow register in Sone is toggled, it merely results in an ACK being returned to the other system, so the shadow-shadow register of the other system is toggled.

In addition, Sone is completely silent as to a mask mechanism of the current system that is switched to a first or second state when the register indicates a specific value and a transmission mechanism that transfers the output from the mask mechanism. Merely transferring an ACK to the other system when the shadow register is toggled, which results in the toggling of a shadow-shadow register of the other system, is not a switching an output state of an output means when a switching control means, i.e., a register, indicates a predetermined value or another value. The register of the present invention switches the output state of the mask mechanism such that the switched output state can be transferred. Sone does not suggest that any of the cited registers switch an output state of a mask mechanism such that the switched output state is transferred to the other system. Sone further does not suggest a switching and controlling means which is composed of a register and a switching and outputting means composed of a mask mechanism that switches to a first state when the register has a predetermined value and switches to a second state when the register has another value, where the switching and outputting means switches between a first state where the signal state transmitted by the output means in the other system is output and a second state where negate state is output, and outputting the switched state, as recited in amended claim 4.

Therefore, as Sone does not discuss or suggest "switching control means for switching an output state of said output means," and "switching and controlling means for switching the output said switching and outputting means," does not suggest "output means for switching between a first state in which the system outputs a signal state of the wired OR signal line and a second state in which the system outputs a negate state of the wired OR signal line, and outputting either state to the other system," and "switching and outputting means for switching between the first state where the signal state transmitted by the output means in the other system is output and the second state where negate state is output, and outputting the switched state," and does not discuss or suggest that "said switching control means comprises a register controlled by a processor in the system, and said output means comprises: a mask mechanism which switches to said first state when the register indicates a predetermined value and which switches to the second state when the register indicates another value; and a transmission mechanism that transfers an output from said mask mechanism to the other system," and that " said switching and controlling means is composed of a register controlled by a processor in the system, and said switching and outputting means is composed of a mask mechanism which switches to the first state when said register has a predetermined value and switches to the second state when the register has a value other than the predetermined value," as recited in amended independent claims 2 and 4, claims 2 and 4 patentably distinguish over the reference relied upon. Accordingly, withdrawal of the § 102(b) rejection is respectfully requested.

Claims 5 and 6

Sone further does not discuss or suggest:

> switching the wired OR signal line in one of the systems to the asserted state if the wired OR signal line of one of the systems is brought into the asserted state, when each of the output means is in the first state;
>
> processing a device that has brought the wired OR signal line in said other system into the asserted state, after the switching; and
>
> switching each of said output means to the second state, verifying the negate state of the wired OR signal lines in the two systems, and then switching each of said output means to the first state,

as recited in independent claim 5, and does not discuss or suggest:

> switching the wired OR signal line in one of the two systems to the asserted state if the wired OR signal line of the other system is brought into the asserted state, when each of the switching and outputting means is in the first state;
>
> processing a device that has brought the wired OR signal line in said other system into the asserted state, after the switching; and

> switching each of said switching and outputting means to the second state, verifying the negate state of the wired OR signal lines in the two systems, and then switching each of said switching and outputting means to the first state,

as recited in independent claim 6.

The Examiner alleges that processing a device is interpreted by the Examiner as servicing the device's [the peripheral adapter's] interrupt request and that "i.e., executing a corresponding interrupt service routine in Sone is considered equivalent to processing a device in the current application". The Examiner then alleges that after the processing of the device has finished, switching the output means to the second state, verifying the negate state, and then switching the output means to the first state corresponds to Sone in which "i.e., the -IRQn line starts at the high state in both devices while running a process, then switches to the low state [see time marker A] after finishing the currently running process in order to service the Interrupt handling routine." Figure 20 describes the process involving the primary system, but does not show or discuss that, after the switching of the signal line in one system to the asserted state if the wired OR signal line one of the system is brought into the asserted state, a device that has brought the wired OR signal line in the other system into the asserted state is processed, and switching each of the output means to the second state, verifying the negate state in both systems, and switching each of the output means to the first state, as recited in claims 5-6.

The Examiner cites Figure 20 as switching from the high state to the low state after finishing the currently running process (time marker A). However, Sone does not discuss switching the wired OR signal line to the asserted state when the output means or switching and outputting means is in the first state (i.e., the low state), processing a device after the switching, and after finishing the processing of the device, switching the output means or switching and outputting means to the second state, verifying the negate state, then switching the output mean or switching and outputting means to the first state, as recited in claims 5-6. Sone shows in Fig. 20 that the -IRQn line switches to the low state at time marker A, but does not discuss or suggest that after the device is processed, the output means or switching and outputting means is switched to the second state in which the system outputs a negate state, verifying the negate state, then switching the output means or switching and outputting means to the first state. The Examiner interrupts servicing the device's interrupt request as processing a device, but does not then show how, after the processing, the output means is switched to the second state indicating a negate state, verifying the negate state of the wired OR signal lines of both systems then switching the output means to the first state.

Therefore, as Sone does not discuss or suggest all the features of independent claims 5 and 6, claims 5 and 6 patentably distinguish over the reference relied upon. Accordingly, withdrawal of the § 102(b) rejection is respectfully requested.

Conclusion

In accordance with the foregoing, claims 2 and 4 have been amended. Claims 1, 3 and 7-9 have been cancelled. Claims 2 and 4-6 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

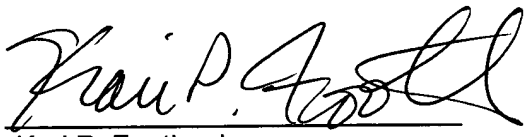
Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 8/9/06

By: 

Kari P. Footland
Registration No. 55,187

1201 New York Avenue, NW, 7th Floor
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501